



# UNITED STATES PATENT AND TRADEMARK OFFICE

CP

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,594	03/25/2004	Van Hoa Lee	AUS920040058US1	7104

35525 7590 10/13/2006

IBM CORP (YA)  
C/O YEE & ASSOCIATES PC  
P.O. BOX 802333  
DALLAS, TX 75380

EXAMINER

GU, SHAWN X

ART UNIT	PAPER NUMBER
----------	--------------

2189

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/809,594	<b>Applicant(s)</b> LEE, VAN HOA	
	<b>Examiner</b> Shawn Gu	<b>Art Unit</b> 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 September 2006.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-16,18-25 and 27-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-3,5-7,9-12,14-16,18-21,23-25 and 27-30 is/are rejected.  
7) ☒ Claim(s) 4,13 and 22 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This final Office action is in response to the amendment filed 1 September 2006. Claims 1-7, 9-16, 18-25 and 27-30 are pending. Claims 8, 17 and 26 are cancelled. New claims 28-30 have been added. All objections and rejections not repeated below are withdrawn.

### ***Claim Objections***

2. Claims 28-30 are objected to because of the following informalities:  
  
Per claims 28-30, the acronym "DMA" should be spelled out as "Direct Memory Addressing" as the acronym is first mentioned in these claims.  
  
Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2189

4. Claims 1-3, 5, 6, 10-12, 14, 15, 19-21, 23, 24 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawkins et al. [US 2002/0124194 A1] (hereinafter "Dawkins").

Per claims 1, 10 and 19, Dawkins teaches a method in a data processing system for providing valid translation entries in a translation control entry table (TCE facility and TCE Table, see Pg. 4, Para. [0043], [0044], [0046]) for all supported direct memory addresses, comprising:

reserving a page in system memory ("a reserved page per image ... ", see Pg. 4, Para. [0046]) for form a reserved page (the reserved page clearly must be formed first before being pointed to);

writing the reserved page (a page of memory is written to when a write operation from the operating systems addresses a memory range within the page);

selecting a region in system memory for the translation control entry table (the TCE table must be stored somewhere in system memory for the Hypervisor and the operating systems to access it, see Pg. 4, Para. [0046]); and

initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page ("initializes all entries in ... TCE table to point to a reserved page ... ", see Pg. 4, Para. [0044] and [0046]).

It is also clear the data processing system of claim 10 is already substantially disclosed above, as well as the computer program product in a recordable-type medium ("software", see Pg. 5, Para. [0050] and [0051]; "computer instructions", see Pg. 6, Para.[0066], [0068], [0076] and Pg.7, Para.[0077]) of claim 19.

Per claims 2, 11 and 20, Dawkins further teaches updating an entry in the translation control entry table, wherein a physical memory page replaces the reserved page when the entry is used by an operating system's device driver (TCE mapping with I/O adapter DMA range, see Pg. 4, Para. [0047] and [0048]).

Per claims 3, 12 and 21, Dawkins further teaches restoring the entry in the translation control entry table with the reserved page when the entry is no longer used by an operating system (reserving the page is done during platform initialization, at which point the previous mapping by an operating system must be replaced by the page reservation, see Pg. 4, Para. [0046]).

Per claims 5, 14 and 23, Dawkins further teaches the page in the system memory and the reserved page are inaccessible to an operating system running on the data processing system (the reserved page is owned by an OS image, not by "one of the other OS images", see Pg. 4, Para. [0046]).

Per claims 6, 15 and 24, Dawkins further teaches writing the reserved page includes setting all bytes within the reserved page to 0xFF (reserving a page implies initializing the page, therefore the byte values within the reserved page are arbitrarily set to known values. Setting all bytes to 0xFF is merely a design choice).

Per claims 28-30, Dawkins further teaches the reserved page is utilized for DMA address translation (Page 4, Paragraphs [0041], [0046] and [0047]).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 7, 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins et al. [US 2002/0124194 A1] (hereinafter "Dawkins"), in further view of Tanenbaum et al. [Operating Systems: Design and Implementation] (hereinafter "Tanenbaum").

Per claims 7, 16 and 25, Dawkins does not specifically teach setting all valid bits to "1". However, Tanenbaum teaches an address translation mechanism (TLB, see Tanenbaum, Pg. 328, Fig. 4-12) that sets valid bits of its table entries to "1" to indicate the entries are valid (in use, see Pg. 328, Ln. 20-21). Since Dawkins initializes its TCE table entries to contain the address of the reserved page as described in claim 1, the entries are in use and therefore valid. Hence, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to associate valid bits to the table entries and set the bits to "1" to indicate that the entries are valid (in use).

Art Unit: 2189

7. Claims 9, 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawkins.

Per claims 9, 18 and 27, Dawkins does not specifically teach the size of the TCE table, the number of table entries, or the size of the table entries. However, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that these specific values are dictated by design choices and system parameters such as the size of system memory, page size, addressing format and performance costs.

#### ***Allowable Subject Matter***

8. Claims 4, 13 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Arguments***

9. Applicant's arguments filed on 1 September 2006 regarding claims 1-7, 9-16, 18-25 and 27-30 have been considered but they are not persuasive. The newly added limitations are taught by Dawkins et al. [US 2002/0124194 A1], in further view of Tanenbaum et al. [Operating Systems: Design and Implementation], as set forth above.

Art Unit: 2189

10. Regarding the Applicant's first argument (see Remarks, Pg.8, para.1), the Applicant states that "Dawkins does not teach 'writing the reserved page and initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page'". The Applicant further states that Dawkins does not teach these limitations because Dawkins does not verify that the reserved page is actually valid (see Remarks, Pg.9, para.1). However, verifying the entries is not a claimed feature of the invention, and the independent claims merely recite "... all entries are initialized to be valid ...". The Examiner interpreted the claims without considering the specific detail described in the specification (see specification, pg.11) about how the entries are initialized to be valid and rejected the claims accordingly. To one ordinarily skilled the art, the TCE entries initialized by Dawkins' hypersivor to point to a reserved page owned by an OS image in order to prevent errors caused by unauthorized accesses are considered to be valid (see Dawkins, pg.4, para.[0046]. The Applicant must recite the features in the claims in order for them to be considered. The Applicant also argued that the initialization step is not inherently anticipated by Dawkins because this step is not necessarily present (see Remarks, pg.10, para.1), although the Examiner presented clear evidence that Dawkins explicitly, not inherently teaches this step as set forth in claims 1, 10 and 19's rejections. What is not necessarily present in the Applicant's admitted prior arts (see specification, pg.16, para.1) is clearly present in Dawkins' teaching.

As for the argument that Dawkins does not teach "writing the reserved page", it should be clear that Dawkins' reserved page is owned and accessed by an OS image



and an I/O adapter for DMA operations, and the page must be written (see Dawkins, pg.4, para.[0046]-[0047]) as memory operations include write operations (data read from the page must be written into the page first).

Regarding the Applicant's second argument (Remarks, pg.12, last two paragraphs) that claim 19 is not taught by Dawkins, it should be clear that claim 19 is already substantially described by claims 1 and 10, except claim 19 recites a computer program product in a recordable medium comprising instructions to perform the recited steps and features of claims 1 and 10. In addition to the reference paragraphs cited in the previous office action, Dawkins further teaches that its invention is capable of being distributed in the form of a computer readable medium (i.e. RAM, CD-ROMS, DVD-ROMSs) of instructions (see Dawkins, pg.7, para.[0077]). It clearly indicates that Dawkins anticipates claim 19.

Regarding the Applicant's third argument (see Remarks, pg.14-15, section VI.B), the Applicant argued that Dawkins and Tanenbaum cannot be combined because they are directed to distinct problems. However, Dawkins already describes initializing entries TCE table. Dawkins does not teach how to indicate/mark an entry as valid, but it clearly indicates a motivation for a method to determine the status of the entries. Tanenbaum's teaching, although not in the exact same topic as Dawkins', offers a well-known method of marking entries with "0" and "1" bits to indicate their status. Such a teaching does not deviate from the field of digital logic design, which is an area related

Art Unit: 2189

to Dawkins' step of initializing TCE table entries. Determining how to initialize TCE table entries and initialize page table entries both direct to the problem of how to digitally mark a data table entry using binary values in a digital computing system. There is clearly sufficient motivation for the combination of Dawkins and Tanenbaum.

The Applicant did not present further arguments regarding the other dependent claims other than stating that the claims are patentable due to the patentability of the independent claims. The dependent claims therefore stand rejected.

11. No new ground of rejection is presented by the Examiner in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2189

**Conclusion**

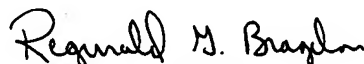
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shawn X Gu  
Assistant Examiner  
Art Unit 2189

  
REGINALD BRAGDON  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100

7 October 2006